Test data requirements for assessment of alternative Pb-free solder alloys

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Since the implementation of EU RoHS in 2006, the electronics industry has seen a proliferation of Pb-free alloys for wave soldering, mini-pot rework, BGA and CSP solder balls and, more recently, solder pastes for mass reflow. New alloys may help reduce cost; however, the risk of reduced thermal fatigue life, improper soldering with high melting point alloys, laminate damage due to high solder pot temperatures and other potential negative effects present challenges and possible field reliability risks for OEMs.

The authors have defined a set of tests that can be used for assessing new SnAgCu, SnAg and SnCu alloys for general use in electronics. The goal of this protocol is to standardize the test methods, test parameters, test vehicles and control samples so that the performance of each new alloy can be properly and fairly assessed relative to previously studied materials. These tests represent the minimum data required, and additional tests may be needed for special applications.

Keywords: Pb-Free Solder Alloy, SAC Family, Thermal Fatigue Life, Field Reliability

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Introduction

The standardization on near-eutectic SnAgCu alloys for Pb-free electronics was instrumental in enabling the electronics industry to meet the requirements of EU RoHS legislation by 1 July 2006. The SAC family of alloys, which includes Sn-3.0Ag-0.5Cu, Sn-[3.5-3.6]Ag-[0.7-0.9]Cu (eutectic), Sn-3.9Ag-0.6Cu (iNEMI) and Sn-4.0Ag-0.5Cu, has proven to be an acceptable, working solution for a broad range of applications.

Nevertheless, it is clear that these materials, while functional, are not ideal. The short RoHS transition period did not allow sufficient time for systematic alloy design and testing to identify optimal SnPb replacements.

When screening began in earnest to find Pb-free alloys to meet the RoHS deadline, many alternatives to SnPb had already been developed both in universities and in industry. However, the long dominance of SnPb meant that many of the widely available alternatives were specialty alloys developed for applications where SnPb was inappropriate, rather than replacement technologies intended to surpass SnPb performance.[1-4]

In the years since the RoHS deadline, the industry has had an opportunity to revisit the formulations of Pb-free solders, and a wide range of new alloys has been developed.[5-24]

A significant obstacle to useful, data-driven assessments of alternate Pb-free alloys has been the inconsistent testing that has been performed on the materials. The data from experiments conducted on these newer materials, while valid on their own, are often not comparable in any meaningful way to data from other equally valid experiments due to the choice of test conditions, controls, or other parameters. Also, alloys formulated to meet specific goals, such as improved mechanical shock resistance, have not always been tested to determine suitability for general use by assessing other performance aspects, such as thermal fatigue life.[25-28]

A range of tests has been included in this protocol in order to provide a balanced assessment of potential alloys. If widely adopted, the standardized test protocol presented in this paper would help bridge the gap between the specialized data generated on materials optimized for particular attributes and the data required for assessing the suitability of alloys for general use. This test protocol does not completely eliminate validation tests needed for special applications; however, it should significantly reduce duplicate testing and improve the quality of the primary reported data for new materials.

Accepteance criteria

This assessment approach only establishes the tests and data reporting, not the acceptance criteria for alloys. This point is important because pass/fail criteria may vary by industry segment, by company and by product. However, the underlying data needed to evaluate new alloys are likely to be similar in most cases. Thus, the assessment method provided in this paper is believed to be relevant across the entire electronics industry.

Controls

Most tests in this protocol have an alloy or combination of alloys specified as controls. These controls have been selected to allow for ordered ranking against currently accepted materials. By bounding the performance of new materials with the current and historic materials of SAC alloys and SnPb, appropriate pass/fail criteria are often apparent.

For example, both SAC305 and SnPb controls are required in accelerated thermal cycling (ATC). It is possible that low silver alloys may not perform as well as high silver alloys in ATC, however, some may be comparable to or better than SnPb. If low silver alloys were only compared to high silver SAC alloys, they might be rejected due to the unfavorable comparison in ATC despite having acceptable performance when compared to SnPb. If they were only compared to SnPb, there would be no direct assessment against the current solution. By comparing the new alloy against both high silver SAC and SnPb controls, the acceptance criteria can be set with respect to historical performance of a well known material in addition to the current solutions.

In many cases, reasonable simplifications were made in selecting controls and variables in an effort to reduce the number of tests and combinations. For example, a wide variety surface finishes are available, however, in some tests the number of finishes was narrowed based on the intermetallic compounds (IMC) formed or based on known failure modes. For example, in mechanical shock testing, NiAu and OSP were chosen as surface finishes because they form the two IMCs of interest and because NiSn intermetallics have been associated with sporadic, low stress fractures in joints made with high silver SAC alloys.

Another significant benefit of selecting control alloys is that they ensure the integrity of the tests by allowing comparison to published literature.

Contamination reports

A central feature of this protocol is that most tests require complete contamination reports on the actual materials used and not only on a representative sample. This requirement was established because many of the new alloys have been designed to include very low-level additions of dopants, which serve as active contributors to the functionality of the materials.

Since most alloys with dopants have been patented based on claims that the additions make the solder different enough from existing materials to warrant IP protection, the logical conclusion is that these dopants must be accounted for in all tests, even when the additions would have been considered contaminants rather than a functional part of the composition in the past. Only complete contamination reports on actual tested material will allow the fair comparison of alloys and the identification of sources of confounding results, should functional levels of dopants be present as contaminants.

Tests and reporting

The required tests are divided into three major areas:

- Reliability
- Manufacturability
- Material properties

The complete set of tests and parameters is shown in *Table 1*. These detailed tests and procedures, as well as test board designs, will be reflected in HP specifications for qualifying solder paste alloys, wave solder and minipot rework alloys and BGA/CSP ball alloys.

It is important to note that the goal of these tests is the assessment of the solder, not the laminates, surface finishes, or equipment capability. Many typical tests that may be found in other assessments have been excluded or structured differently than traditional process optimization experiments in order to remain focused on the alloy.

Although the number of tests, combinations, controls and samples may seem overwhelming at first, these tests were actually selected from a much longer list of potential tests. This set of tests was viewed as the minimum set required to generate sufficient information to assess the suitability of a high Sn solder in the SnAgCu, SnAg, or SnCu families intended for use in high volume manufacturing of electronics. It is unlikely that a single supplier will complete all portions of the testing alone, but rather partners with appropriate capabilities will probably collaborate to generate the data for a material.

> *"A significant obstacle to useful, data-driven assessments of alternate Pb-free alloys has been the inconsistent testing that has been performed on the materials."*

Reliability

Mechanical and thermal fatigue reliability tests are the primary tests required for any new alloy. Many reliability tests can be used to evaluate alloys, but four key tests were chosen as the most critical for surface mount solder alloys:

- Accelerated thermal cycling (*IPC-9701-A*, TC1)
- Mechanical shock (*JESD22-B111*, Condition B)
- Vibration (*IEC 60068-2-64*)
- Four point bend (*IPC-9702*)

Daisy-chained components and the use of continuous monitoring during testing are essential for these evaluations and are required for all surface mount alloy reliability tests. Reworked samples have not been specified for these four tests, as the requirement for properly reworked joints is that they meet the same requirements as for as-formed joints. Standardized board designs for these tests are being finalized and will be included in the HP alloy qualification specifications that will be publicly released in 2008.

TC1 (0°C to 100°C) is the default condition for accelerated thermal cycling (ATC), although TC2 (-25°C to 100°C) is an acceptable alternative. The disadvantage of the smaller ΔT in TC1 as compared with other test conditions is outweighed by the widespread use of the 0 to 100°C cycle in TC1, which makes data generation, collection and comparison easier.

Multiple thermal cycle conditions have not been specified in this assessment. Although multiple conditions are required in developing acceleration models, it was not considered strictly necessary to assess performance in multiple test conditions to make reasonable decisions on the suitability of an alloy. Of course, further work would be needed to fully characterize and model a new alloy.

Combinations of alloys and solder balls have been selected to evaluate the compatibility of new alloys with existing technologies. For example, new paste alloys are evaluated using BGAs with SAC105 balls in ATC and with BGAs with SAC405 balls in shock, vibration and bend. These cases are likely to occur in common applications and problems with these combinations would indicate potential compatibility issues with currently available technologies. No acceptance criteria have been specified and specific applications designed without these alloy combinations might be able to use a material that showed poor results in these tests. However, it is desirable to identify compatibility issues wherever possible, even when it is not a formal criterion for acceptance.

Table 1. Summary of test methods, parameters, controls, and reporting requirements for the assessment of new Pb-free solder alloys.

Reliability

Test and method	Test parameters	Control(s)	Report
Accelerated thermal cycling *IPC-9701-A* Solder paste and BGA/CSP ball alloys	**Test condition:** TC1 (0°C to 100°C) with 10 minute ramps and 10 minute dwells, 6000 cycles or failure of all components, whichever occurs first. **PCB**: HP standardized test board, 0.093 inches thick, six layers, 1/2 oz copper foil, OSP surface finish, non solder-mask defined (metal-defined) pads for area array components **Components**: Standardized BOM with BGAs andTSOPs, with silicon die and daisy chains as per *IPC-9701-A* • Type II TSOPs with Fe-Ni Alloy 42 leads • BGAs with 1.27 mm or 1.0 mm pitch • BGAs in the following combinations: 1. SnPb ball alloy and SnPb paste 2. SAC305 ball alloy and SAC305 paste 3. New alloy ball and new alloy paste 4. Different combinations depending on material: a. If evaluating solder paste alloy, test combination of SAC105 alloy ball and new alloy paste b. If evaluating BGA /CSP ball alloy, test combination of new alloy ball and SAC105 paste **Samples**: 32 of each alloy combination **Preconditioning**: Test boards must be placed in an oven within 24 hours of assembly and baked in air at125°C for 48 hours for lead-free and 24 hours for the tin-lead boards, and then tested within one week.	SnPb, SAC305, SAC105	Weibull curves for each alloy combination. Tabulated failure data for each alloy combination. Thermal profile used for testing.
Mechanical shock *JESD22-B111* Solder paste andBGA/CSP ball alloys	**Test Condition**: B, 1500 G, 0.5 ms duration, half-sinepulse. **PCB**: HP standardized test board as per Section 5.2, 1 mm thick, eight layers, 1+6+1 build-up, both OSP and electrolytic Ni/Au (not ENIG), non solder-mask defined (metal-defined) pads **Components**: Standardized BOM with area arrays with silicon die and daisy chains as per *JESD22-B111*, no PTH or leadframe components, package surface finish OSP or SOP, two types of components: 0.50 mm and 1.0 mm pitch (no larger than 15 mm x 15 mm), BGAs/CSPs in the following combinations: 1. SnPb ball alloy and SnPb paste 2. SAC405 ball alloy and SAC405 paste 3. New alloy ball and new alloy paste 4. Different combinations depending on material: a. If evaluating solder paste alloy, test combination of SAC405 ball and new alloy paste b. If evaluating BGA/CSP ball alloy, test combination of new ball alloy and SAC405 paste **Samples**: Test 32 components for each combination of finish, pitch, ball and paste alloy PCB finish (OSP and Ni/Au) and for each of the four combinations of reflow alloy and ball alloy, for a total of 512 components. Four components on each test board, each combination of PCB finish, pitch, and alloy require eight boards, for a total of 128 boards. **Preconditioning**: Test boards must be placed in an oven within 24 hours of assembly and baked in air at125°C for 48 hours for lead-free and 24 hours for the tin-lead boards, and then tested within one week.	SnPb, SAC405	Report as per Section 8 of *JESD22-B111* for all test conditions, including eight Weibull curves (one for each surface finish and alloy combination). Tabulated failure data for all four alloy combinations for both surface finishes, as specified in section 7 of *JESD22-B111*. Reflow profile from the test vehicle assembly.
Vibration *IEC 60068-2-64* Solder paste andBGA/CSP ball alloys	**Test condition**: Method 2, with sweeps for the discovery of resonant points. **PCB**: Same as mechanical shock test board, 1 mm thick, eight layers, 1+6+1 build-up, both OSP and electrolytic Ni/Au (not ENIG), non solder-mask defined (metal-defined) pads **Components**: Same as mechanical shock, area arrays with silicon die and daisy chains as per *JESD22-B111*, no PTH or leadframe components, package surface finish OSP or SOP, two types of components: 0.50 mm and 1.0 mm pitch (no larger than 15 mm x 15 mm), BGAs/CSPs in the following combinations: 1. SnPb ball alloy and SnPb paste 2. SAC405 ball alloy and SAC405 paste 3. New alloy ball and new alloy paste 4. Different combinations depending onmaterial: a. If evaluating solder paste alloy, test combination of SAC405 ball and new alloy paste b. If evaluating BGA/CSP ball alloy, test combination of new alloy ball and SAC405 paste **Samples**: Test 32 components for each combination of finish, pitch, ball and paste alloy PCB finish (OSP and Ni/Au) and for each of the four combinations of reflow alloy and ball alloy, for a total of 512 components. Four components on each test board, each combination of PCB finish, pitch, and alloy require eight boards, for a total of 128 boards. **Preconditioning**: Test boards must be placed in an oven within 24 hours of assembly and baked in air at125°C for 48 hours for lead-free and 24 hours for the tin-lead boards, and then tested within one week.	SnPb, SAC405	Report for all test conditions, as per *IEC 60068-2-64*, including: • Initial inspection results • Response graphs indicating the stress applied (power density charts) • Resonant frequencies • Dwell time at each resonant frequency • Results from final inspection • Test observations • Photographs of failed samples • Comparison of performance found between new alloy and controls • Photographs of the test set-up, with details indicating the mounting of the test vehicle to the vibration table • Location of accelerometers • Type of test equipment used (hardware and software) • Calibration records of the test equipment

Test and method	Test parameters	Control	Report
Four-point bend *IPC-9702* Solder paste and BGA/CSP ball alloys	**Test condition**: as per *IPC-9702*, support span at least 20 mm longer than the load span; select the exact value to obtain a strain rate of 5000 με/s (*IPC-9702*, Figure A.1) **PCB**: HP standardized test board conforming to *IPC-9702*, *Section 8.3*, 1 mm thick, 8 layers, 1+6+1 build-up, both OSP and electrolytic Ni/Au (not ENIG), non solder-mask defined (metal-defined) pads, Isola 408 **Components**: same as mechanical shock samples, area arrays with silicon die and daisy chains as per *IPC-9702, Section 8.7*, no PTH or lead frame components, package surface finish OSP or SOP, one type of components (no larger than 15 mm x 15 mm), BGAs/CSPs in the same combinations as the vibration test. **Samples**: Eight boards for each surface finish and solder alloy combination (total of 64 boards). Four components shall be mounted on each board, as described in *IPC-9702*. **Strain gauge locations**: Six strain gauges attached to each board, as specified in *IPC-9702*, Figure 8-4. **Failure criterion**: 20% increase in daisy-chain resistance	SnPb, SAC405	• For each combination of PCB finish (OSP and Ni/Au) and for each paste or ball alloy combination, provide the strain [με] at which failure occurs. • Report support span used.
TH joint strength Pin pull test as described in “*Reliability of Partially-Filled SAC305 Through-Hole Joints,*” Holder, et al, APEX 2006 Wave and minipot alloys only	**Test condition:** pin pull/push rate of 1 mm/min. **PCB**: Culebra test board, 0.130 inches thick, 16 layers, Isola 408, OSP Enthone Entek 106HT, three boards per pin finish, assembled in nominal process **Components:** DIMMs **Samples**: Pull or push pins from two DIMM components per board, fifteen pins per component (90 pins per alloy) **Preconditioning**: • 400 g shock performed once per axis (or random vibration 9 Grms), as per IEC 60068-2-64 • Followed by 1000 cycles 0°C to 100°C thermal cycle, as described in IPC-9701A	SAC305	Plot force vs pin-wetted length for both the new alloy and SAC 305 control on the same graph.
Manufacturing			
Test and method	**Test parameters**	**Control**	**Report**
Design of experiment (DOE) for wave solder alloy *HP wave process characterization test method* Wave solder alloy only	**Variables and test conditions**: • Pot temperature (°C): 240, 255, 270, 285, 300 (validated by thermocouple for each temperature) • Contact time (sec): 3, 5, 7 (measured using a Lev-Check) Lambda wave only **PCB**: Culebra test board, 0.130 inches thick, 16 layers, Isola 408 laminate, OSP Enthone Entek 106HT, variation in hole sizes embedded in design **Components**: DIMMs, headers, delay lines, all fully loaded except J2 which is covered with tape (for copper dissolution evaluation) **Flux**: Cookson RF800, datasheet recommended amount **Replicates:** minimum of twice per new and control alloy (five pot temperatures and three contact times, for a total of 30 runs per alloy) **Preconditioning**: PCBs preconditioned with two nominal Pb-free reflow cycles **Locations for TH fill measurement**: J3, DL1, DL2,DL5, DL6, DL7, DL8, DL9, DL10 **TH fill measurement**: Measure on cross-sectioned joints (or 5DX) as an actual measurement in millimeters expressed as pin-wetted length **Locations for copper dissolution measurements**: DL3, DL4, DL11, and DL12 **Copper dissolution measurement**: Measure the remaining copper of the TH pad and knee in cross-sections. J2 is the unpopulated sites for determination of the ‘original’ thicknesses. **Locations for wetting angle measurement, IMC thickness measurement, hot tearing evaluation, and laminate evaluations**: DL line (cross section one row), pin one at J3	SAC305	Provide data for new alloy and controls for all noted locations for all conditions: • Through hole fill results • Copper dissolution results • Wetting angle • IMC thickness • Hot tearing evaluation • Laminate defect evaluation andcopper via cracking evaluation Report equipment and process parameters: • Flux amount applied • Flux application method • Air knife used • Conveyor angle • Solder level (height) • Pump speed • Preheat time and temperature, and how determined Report yield and visual inspection results: • Number of shorts at 10x mag • Results of yield and visual inspection as per *IPC-610*
Design of experiment (DOE) for reflow solder alloy *HP reflow process characterization test method* Solder paste alloy only	**Variables**: • Time above liquidus (TAL) (sec): 30, 65, 100 • Peak temperature (Tp) (°C): 230, 245, 260, 275,290 **PCB**: HP standardized test boards, 0.093 inches thick, Isola 408, 14 layers, OSP surface finish, non solder-mask defined (metal-defined) pads for area array components **Components**: Standardized BOM with BGAs with SAC305 and SAC105, TSOPs with Ni/Pd/Au, Sn, and SnPb finishes; BOM selected to ensure the following combinations: • SAC305 ball alloy and SAC305 paste • new alloy ball and new paste alloy • SAC305 ball alloy and new alloy paste • SAC105 ball alloy and new alloy paste **Flux**: same for both SAC305 and new alloy, optimize preheat temperature to flux **Replicates**: twice (with three TAL levels and five Tp levels, total of thirty runs for each alloy) Copper dissolution measurement: On a cross-sectioned sample, measure the remaining Cu on the SMT pad.	SAC305	Report: • Results and example photos of visual inspection to *IPC-610* • Representative wetting angles at toe and heel fillet (averaged at three locations) • Results and example photos of x-ray inspection (either transmission or x-ray laminography) of BGAs to *IPC-7095* • Cross-section images: a) IMC thickness b) Copper dissolution • Process parameters: a) Solder paste volume b) Flux used in both pastes c) Reflow profiles as verified by thermocouples in joints
Wetting balance *J-STD-003*	**Test**: F1 – Wetting Balance Test: Lead-free Solder **Pot temperature**: 255°C, as per standard for Pb-free alloys **Flux**: standard activated rosin flux #2 for Pb-free alloys **Samples**: 10 new alloy and 10 SAC305 control **Precondition**: 8 hours at 72C/85% R.H. followed by 1 hour bake at 105°C **Test conditions**: Parts immersed at 45 degrees incident to solder pot to a depth of 0.4 mm at 2 mm/sec	SAC305	Provide data for the new alloy and SAC305 controls: • Wetting balance curves showing individual coupon results (not averaged) for each alloy • Contamination reports before an dafter test for both the new alloy and SAC305 control • Test board thickness and features

Table 1 (continued). Summary of test methods, parameters, controls, and reporting requirements for the assessment of new Pb-free solder alloys.

Test and method	Test parameters	Control	Report
Design of Experiment (DOE) for miniport rework alloys and copper dissolution assessment *HP rework process characterization test method* Wave and minipot rework solder alloys only	**Variables and test conditions**: • Pot temperature (°C): 240 , 270, 300 (validated by a thermocouple at the test setup) • Contact time (sec): 20, 40, 60, 80, 100 (measured with a stopwatch and validated against the machine setting) **Samples**: Culebra PCAs from nominal wave process (see wave DOE above), all components loaded EXCEPT J2, which is taped to protect from soldering in wave, 60 new alloy boards and 60 SAC305 boards **Preconditioning**: prior to wave, precondition PCBs with two nominal Pb-free reflow cycles **Rework component**: J3 256 pin DIMM, remove and replace the J3 connector during a single heat cycle within the 'contact time' variable **Flux**: Cookson OM338PT paste flux, applied immediately before preheat, also applied to new connector pins **Replicates**: two replicates of the 15 conditions for each of the following combinations: • SAC305 wave and SAC305 rework • new alloy wave and SAC305 rework • new alloy wave and new alloy rework • SAC305 wave and new alloy rework **Equipment**: AirVAC PCBRM15 system with computer-controlled time and pre-heater, board support fixtures, and support fixtures that extend into the preheat area **Flow rate**: characterized before the experiment with low and high knob settings at a nominal temperature and time (270°C, 60 sec), then fixed (this requires laminar flow and constant pot [full] level, 1/4 inch from the lip of the pot) **Preheat time and temperature**: Flux before preheat. Board must reach a temperature between 120°C and 130°C. Use instrumented, board-monitoring, board temperature techniques (calibrate using an instrumented assembly with thermocouples on both top and bottom sides) for verification. Using an instrumented board placed over the pot, monitor and record a profile for at least one specific pin using three different thermal energies (profiles at high temperature and time, low temperature and time, and mediumtemperature and time). If possible, try to find the coolest node. **TH fill measurement**: Measure cross-sectioned joints (or 5DX) on J3 as an actual measurement in millimeters expressed as pin-wetted length **Copper dissolution measurement**: Measure the remaining copper of the TH pad and knee in cross-sections on J3. J2 is the unpopulated sites for determination of the 'original' thicknesses.	SAC305	Report: • Through hole fill results and example photos of visual inspection to IPC-610 for J3 • Cross-section images for pin 1, 56, 128, 129, 185, and 256 of J3 • Copper dissolution measurements on cross-sectioned joint samples of J3 as compared to J2 (at pins above) • IMC thickness measurements on cross-sectioned joint samples of J3 (at pins above) • Laminate defect evaluation and copper via cracking evaluation for J3 (at pins above) • Equipment and process parameters: a) Nozzle b) Flow rate c) Sample run order d) Thermal profile
Material Properties			
Property and test method	**Test parameters**	**Control**	**Report**
Liquidus and solidus temperature *DTA or DSC by ASTM E794-06*	As per test method	SAC305	T_L and T_S in °C, and graph of heat flow versus temperature.
Electrical resistivity *ASTM B193-02*	Test at 293°K	None	Electrical resistivity (*p*) in μΩ-cm
Thermal conductivity	Measured or calculated from electrical resistivity test at 293°K	None	Thermal conductivity (*k*) in W/(m-K)
Young's modulus, shear modulus, and Poisson's ratio Ultrasonic stress wave propagation technique by *ASTM 1875-00*	Sample must be a rectangular bar with a length to thickness ratio of 20:1 to 25:1 and a width to thickness ratio of at least 5:1. Use equations (2) and (4) to determine the elastic modulus (E), equation (8) to determine the shear modulus (G), and equation (15) to determine Poisson's ratio (*v*).	SnPb	Measured E and G in GPa, and calculated Poisson's ratio (*v*). Report geometry of test sample.
Stress-strain curve, 0.2% yield strength, ultimate tensile strength,and elongation Tensile testing	**Test conditions**: • Temperature (ºC): -25 (optional), 25, 75, 125, 160 • Rate: 3 mm/min (resulting in strain rate of 10-3 s -1) **Samples**: Three samples of each alloy; bulk solder samples with round gauge sections between 2 mm to 5mm in diameter and gauge length of 50 mm. Geometry and testing conditions must be identical for all samples.	SAC305	Plot the engineering stress vs. engineering strain (to failure), measured by conventional tensile testing for both alloys at each temperature. Average the three samples at each temperature and provide all eight graphs. Report sample gauge diameter in mm.
Density	Direct measurement of volume and mass	None	Density (*p*) in g/cm³
Vickers hardness *ASTM E92-82(2003)e2*	As per test method	None	HV [dimensionless]
Coefficient of thermal expansion (CTE) TMA as per *ASTM E831-06*	**Test condition:** Measurements taken every 25°C from 50°C to 200°C, averaged for the three tests of each solder alloy **Samples**: Three samples of each alloy, 10 mm in length, lateral dimensions not to exceed 5 mm. **Ramp rate**: 10°C/min.	SAC305	Graph of thermal expansion (ppm/ºC) versus temperature (ºC) for new alloy and SAC305. Provide the standard deviation for each data point (as error bars), along with the averaged values at each temperature. Report average CTE between -50°C to200°C in ppm/ºC for each alloy. Report sample shape and dimensions.

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The BGA packages selected for these tests have relatively large pitches (0.5 mm and 1.0 mm). This choice was made in order to focus on the performance of the bulk solder and not force failure modes primarily associated with surface finishes or package types.

With respect to through-hole joints, these four tests (ATC, shock, vibration and bend) are not as useful in completing reliability assessments as they are for assessing surface mount joints. Through hole joints are known to be much more robust than surface mount joints in ATC and mechanical tests and testing to failure would be impractical. So in lieu of these tests, only a pin push or pull test (with ATC, shock and vibration preconditioning) is necessary for reliability assessments of wave and minipot rework alloys.[29]

Manufacturability

The second major area for alloy evaluation is manufacturability. The objective of these experiments is to characterize the complete process window of a new material by determining the impact of time and temperature process settings on important response variables. This information is critical for assessing the suitability of a material for use in high volume electronics assembly. The following tests have been included in the manufacturing assessment for new alloys:

- Wave solder process characterization (HP DOE)
- Reflow process characterization (HP DOE)
- Rework process characterization and copper dissolution assessment (HP DOE)
- Wetting balance (IPC J-STD-003, F1)

Assessing the manufacturability of solder alloys in a reproducible way is challenging because, unlike reliability tests, standard manufacturing test methods and test boards are not available. A wide variety of equipment combinations and processes are used, and reported data are rarely comparable to other tests. In addition, most available data are focused on process optimization and capability assessment, rather than identifying the complete process window.

The goal of the manufacturing tests in this protocol is to characterize the performance of new alloys over their entire process window, not just to identify optimal points. Many alternate alloys can be successful to some degree in highly optimized processes due to the inherent solderability of high Sn alloys. However, alloys with very small process windows may not be robust enough for general use, and characterizing the entire process window is more important in this type of assessment than identifying the existence of single point solutions.

Understanding the process window and behavior over an extended temperature range also helps to gauge the likelihood of processes being run beyond component temperature limits. For example, consider a case in which an alloy yields better results as the temperature increases all the way to very high temperatures. Even if the alloy is capable of soldering at lower temperatures, at least some manufacturers will probably attempt to run the process at the highest temperatures to achieve the highest yield, potentially damaging components. Therefore, characterization of manufacturing performance across the entire process window is needed for alloy assessment. Focusing on characterizing the process window means that some tests in this protocol have more levels in the DOEs than might be used for traditional process optimization. In addition, the range of process temperatures and variables is larger than usual in order to help determine the curvature of the response data. It should be noted that the data from the three inner levels of the five level DOEs can still be used for process optimization.

With respect to the test boards, the reflow test vehicle incorporates component combinations to evaluate the compatibility of new alloys with SAC305 and SAC105. The HP designed Culebra test board was chosen as the test vehicle for the through hole experiments. A single thickness is used for all tests (0.130 inches) because pin wetted length is the measured variable rather than percent hole fill.29 By using pin wetted length as the response variable, results from thick boards can be used to predict behavior for thinner boards.

Material Properties

Many physical properties can be measured for solder alloys; however, not all of them are useful or relevant for assessing the suitability or acceptability of new alloys. Only the liquidus and solidus temperature measurements are considered strictly required in the assessment protocol. Depending on the application, it may be necessary to determine properties in addition to liquidus and solidus temperatures in order to complete comprehensive engineering evaluations. For example, the stress-strain and elastic properties of the alloys are needed if finite element analysis is to be performed.

The following tests generate data on basic material properties that may be useful for assessing material suitability:

- Liquidus, solidus temperatures (ASTM E794-06)
- Electrical resistivity (ASTM B193-02)
- Thermal conductivity
- Young's modulus, shear modulus and Poisson's ratio (ultrasonic stress wave propagation technique by ASTM 1875-00)
- Stress-strain curve, 0.2% yield strength, ultimate tensile strength and elongation (tensile testing)
- Density
- Vickers hardness (ASTM E92-82(2003)e2)
- Coefficient of thermal expansion (CTE) (ASTM E831-06)

Determining some material properties may be considered optional in the case of evaluating SnAgCu, SnAg and SnCu alloys because of the expected similarity with known materials. However, if this assessment approach is extended to materials beyond these alloy families, all tests should be required.

Conclusion

This paper presents a core framework of tests that can be used to evaluate and compare alternative Pb-free alloys based on the reliability, manufacturability and material properties of the alloys. Detailed test definitions and reporting requirements have been established in order to enable meaningful data comparisons between alloy tests. This protocol is appropriate for evaluating SnAgCu, SnAg and SnCu alloys for use in electronics.

These tests will be reflected in HP specifications that will be publicly released in 2008 for the qualification of solder paste alloys, wave solder and minipot rework alloys and BGA/CSP ball alloys, although minor adjustments may be made as test boards and BOMs are finalized.

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